IN THE CLAIMS

1. - 22. (Cancelled)

23. (Previously Presented) An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising:

a read transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse during an active mode; and

a latch circuit to latch a state of the antifuse during a sleep mode.

24. (Previously Presented) The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference; and

the read transistor comprises a p-channel transistor having a source terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a drain terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors.

25. (Withdrawn) A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a read transistor;

detecting a voltage of the second terminal of the antifuse to read the antifuse during an active mode; and

latching the voltage of the second terminal of the antifuse during a sleep mode.

26. (Withdrawn) The method of claim 25 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel read transistor switched on by a bias voltage;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode; and

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter during a sleep mode.

27. - 33. (Cancelled)

34. (Original) The antifuse circuit of claim 23 wherein:

the read transistor comprises a p-channel read transistor having a source terminal coupled to the read voltage and a gate terminal coupled to a bias voltage;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising a p-channel transistor coupled between the read transistor and the second terminal of the antifuse that is switched on when the antifuse is being read.

35. (Original) The antifuse circuit of claim 23, further comprising:

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode;

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference;

a floating well driver logic circuit coupled to a gate terminal and a well of a p-channel transistor in the read circuit or the latch circuit to raise a voltage of the gate terminal and the well during the programming mode to substantially prevent current in the p-channel transistor; and

wherein the read circuit further comprises a plurality of p-channel transistors, one of the p-channel transistors being coupled between the second terminal of the antifuse and the floating well driver logic circuit to couple a rising voltage on the second terminal of the antifuse to the floating well driver logic circuit.

36. (Original) The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises an n-channel transistor having a drain terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a source terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of n-channel latch circuit transistors and an output coupled to gate terminals of the n-channel latch circuit transistors; and

further comprising an n-channel transistor coupled between the read transistor and the second terminal of the antifuse that is switched on when the antifuse is being read.

37. (Original) The antifuse circuit of claim 23 wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

38. (Original) The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising n-type material, the first terminal being coupled to a voltage source;

the read transistor comprises a long-L n-channel transistor having a source terminal coupled to a ground voltage reference, a gate terminal coupled to a bias voltage, and a drain terminal coupled to the second terminal of the antifuse; and

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors.

39. (Withdrawn) The method of claim 25 wherein:

coupling a read voltage further comprises coupling the read voltage to the second terminal of the antifuse through a p-channel read transistor switched on by a bias voltage during the active mode;

detecting a voltage further comprises detecting the voltage of the second terminal of the antifuse with an input of an inverter during the active mode;

latching the voltage further comprises latching the voltage of the second terminal of the antifuse with a latch circuit comprising the inverter coupled to a plurality of latch transistors; and

further comprising switching on a p-channel transistor coupled between the read transistor and the second terminal of the antifuse during the active mode.

40. (Withdrawn) The method of claim 25, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode;

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse; and

switching off transistors in a read circuit coupled to the antifuse during the programming mode with a floating well driver logic circuit coupled to the read circuit by raising a voltage of a gate terminal and a well of a p-channel transistor to substantially prevent current in the p-channel transistor.

41. (Withdrawn) The method of claim 25 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode; and

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of n-channel latch transistors during a sleep mode.

42. (Withdrawn) The method of claim 25 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

43. (Withdrawn) The method of claim 25 wherein:

coupling a reference voltage comprises coupling a voltage source to a first terminal of an antifuse, the first terminal comprising n-type material;

coupling a read voltage comprises coupling a ground voltage reference to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage, the second terminal comprising n-type material;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter; and

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch circuit transistors.

44. (Currently Amended) An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage, the reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising:

a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse; and

an inverter having an input coupled to the second terminal of the antifuse.

45. (Currently Amended) ~~The antifuse circuit of claim 44~~ An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse, wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the transistor comprises a p-channel transistor having a source terminal coupled to the read voltage and a gate terminal coupled to a bias voltage; and

the read circuit further comprises an inverter having an input coupled to the second terminal of the antifuse.

46. (Currently Amended) ~~The antifuse circuit of claim 44, further comprising:~~ An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal;

a read circuit to read the antifuse, the read circuit comprising a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse;

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode;

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference;

a floating well driver logic circuit coupled to a well of a p-channel transistor in the read circuit to raise a voltage of the well during the programming mode to substantially prevent current in the p-channel transistor; and

wherein the read circuit further comprises a plurality of p-channel transistors, one of the p-channel transistors being coupled between the second terminal of the antifuse and the floating well driver logic circuit to couple a rising voltage on the second terminal of the antifuse to the floating well driver logic circuit.

47. (Currently Amended) ~~The antifuse circuit of claim 44~~ An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse, wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

48. (Withdrawn) A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a transistor; and

detecting a voltage of the second terminal of the antifuse to read the antifuse, the second terminal coupled to an input of an inverter.

49. (Withdrawn) The method of claim 48 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel transistor switched on by a bias voltage; and

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of [[an]] the inverter.

50. (Withdrawn) The method of claim 48, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode;

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse; and

switching off a p-channel transistor in a read circuit coupled to the antifuse during the programming mode with a floating well driver logic circuit coupled to the read circuit by raising a voltage of a well of the p-channel transistor to substantially prevent current in the p-channel transistor.

51. (Withdrawn) The method of claim 48 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

52. (Original) An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal;

a read circuit to read the antifuse, the read circuit comprising:

a read transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse during an active mode; and a latch circuit to latch a state of the antifuse during a sleep mode; and

a pass-gate device coupled between the antifuse and the read circuit.

53. (Original) The antifuse circuit of claim 52 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises a p-channel transistor having a source terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a drain terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising a p-channel transistor coupled between the read transistor and the pass gate device that is switched on when the antifuse is being read.

54. (Original) The antifuse circuit of claim 52 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises an n-channel transistor having a drain terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a source terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising an n-channel transistor coupled between the read transistor and the pass gate device that is switched on when the antifuse is being read.

55. (Original) The antifuse circuit of claim 52 wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal

comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

56. (Original) The antifuse circuit of claim 52 wherein the pass-gate device comprises an n-channel pass-gate transistor comprising a gate coupled to the read voltage.

57. (Original) The antifuse circuit of claim 52 wherein the pass-gate device comprises an n-channel pass-gate transistor comprising a gate coupled to a voltage different from the read voltage.

58. (Original) The antifuse circuit of claim 52, further comprising:

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode; and

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference.

59. (Withdrawn) A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a read transistor and a pass-gate device;

detecting a voltage of the second terminal of the antifuse to read the antifuse during an active mode; and

latching the voltage of the second terminal of the antifuse during a sleep mode.

60. (Withdrawn) The method of claim 59 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel read transistor switched on by a bias voltage and a pass-gate device;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode;

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch transistors during a sleep mode; and

further comprising switching on a p-channel transistor coupled between the read transistor and the pass gate device during the active mode.

61. (Withdrawn) The method of claim 59 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage and a pass-gate device;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode;

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch transistors during a sleep mode; and

further comprising switching on an n-channel transistor coupled between the read transistor and the pass gate device during the active mode.

62. (Withdrawn) The method of claim 59, further comprising controlling current flow between the antifuse and the read transistor with the pass-gate device, the pass-gate device comprising an n-channel pass-gate transistor comprising a gate coupled to the read voltage.

63. (Withdrawn) The method of claim 59, further comprising controlling current flow between the antifuse and the read transistor with the pass-gate device, the pass-gate device

comprising an n-channel pass-gate transistor comprising a gate coupled to a voltage different from the read voltage.

64. (Withdrawn) The method of claim 59 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

65. (Withdrawn) The method of claim 59, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode; and

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse.

66. (Original) An integrated circuit comprising:

an antifuse having a first terminal coupled to a common bus line;

a program driver circuit coupled to a second terminal of the antifuse to select the antifuse to be programmed during a programming mode;

means for reading the antifuse during an active mode; and

a latch circuit coupled to the second terminal of the antifuse to latch a state of the antifuse during a sleep mode.